Dependence of Pentacene Crystal Growth on Dielectric Roughness for Fabrication of Flexible Field-Effect Transistors

Hoichang Yang,*,† Chanwoo Yang,‡ Se Hyun Kim,‡ Mi Jang,† and Chan Eon Park*,‡

Department of Advanced Fiber Engineering, Inha University, Incheon 402-751, Korea, and Department of Chemical Engineering, Pohang University of Science and Technology, Pohang 790-784, Korea

ABSTRACT The dependence of pentacene nanostructures on gate dielectric surfaces were investigated for flexible organic field-effect transistor (OFET) applications. Two bilayer types of polymer/aluminum oxide (Al_2O_3) gate dielectrics were fabricated on commercial Al foils laminated onto a polymer back plate. Some Al foils were directly used as gate electrodes, and others were smoothly polished by an electrolytic etching. These Al surfaces were then anodized and coated with poly(α-methyl styrene) (PAMS). For PAMS/Al_2O_3 dielectrics onto etched Al foils, surface roughness up to ~1 nm could be reached, although isolated dimples with a lateral diameter of several micrometers were still present. On PAMS/Al_2O_3 dielectrics (surface roughness >40 nm) containing mechanical grooves of Al foil, average hole mobility (μ_{FET}) of 50 nm thick pentacene-FETs under the low operating voltages ($|V| < 6$ V) was ~0.15 cm^2 V^{-1} s^{-1}. In contrast, pentacene-FETs employing the etched Al gates exhibited μ_{FET} of ~0.39 cm^2 V^{-1} s^{-1}, which was comparable to that of reference samples with PAMS/Al_2O_3 dielectrics onto flat sputtered Al gates. Conducting-probe atomic force microscopy and two-dimensional X-ray diffraction of pentacene films with various thicknesses revealed different out-of-plane and in-plane crystal orderings of pentacene, depending on the surface roughness of the gate dielectrics.

KEYWORDS: pentacene • field-effect transistor • conducting AFM • surface roughness • X-ray diffraction

1. INTRODUCTION

Organic field-effect transistors (OFETs) have been intensively studied as potential alternatives to conventional inorganic-based OFETs for electronic applications with low cost, large area, and flexibility (1−5). On smooth hydrophobic dielectrics, seeding pentacene grows into a terracelike crystal layer, providing a high hole mobility (μ_{FET}) in OFETs (6−13). Pentacene-based OFETs are candidates for realizing flexible OFETs with low-cost processing advantages. These OFETs may contain a dielectric layer with a nanoscale rough surface and sputtered or laminated metal gate electrodes. Therefore, understanding the dependence of OFET performance on dielectric roughness is necessary for optimizing the performance of these OFETs.

In general, the hole mobility in top-contact electrode OFETs with pentacene films decreases significantly with increasing dielectric surface roughness, usually defined as the root-mean-square (R_q), for above 1 nm (14−17). We recently reported pentacene-OFETs that operated at low voltages with polymer-coated Al_2O_3 dielectrics ($R_q \approx 1$ nm) on etched commercial Al foil gate, which yielded $\mu_{FET} \approx 0.5$ cm^2 V^{-1} s^{-1} at $|V| < 6$ V (18). In this case, mechanically grooved surface of 50 μm thick Al foil laminated on a polymer backplane could almost be smoothed by electro-

chemical etching, although the polymer-coated Al_2O_3 dielectric still contained the surface trace of etched Al foil with scattered micrometer-sized dimples.

Here we have systematically investigated the dependence of pentacene crystalline structures on gate dielectrics of varying roughness. The structure and extent of π-conjugation within these crystals was also correlated with the electrical performance of OFETs. To control the dielectric surface roughness, we fabricated poly(α-methyl styrene) PAMS/Al_2O_3 bilayer gate dielectrics on three different types of Al gate electrodes: (1) flexible Al foil-laminated poly(ethylene naphthalate) (PEN) before (dielectric **I**) and after (dielectric **II**) electrolytic etching, and (2) rigid sputtered Al/Si substrates (dielectric **III**) (15). Pentacene films of varying thickness were thermally deposited on these gate dielectrics held at room temperature. The resulting films were characterized by atomic force microscopy (AFM) and X-ray diffraction. With top-contact Au electrode OFETs, 50 nm thick pentacene-FETs were operated at low voltages and 5 nm thick pentacene devices were used for conducting-probe AFM (CP-AFM) to evaluate the lateral conductivity along percolated pentacene crystal grains in direct contact with the gate dielectrics. Finally, we showed that the PAMS/Al_2O_3 bilayer dielectrics can be used in high-performance flexible pentacene-OFETs.

2. EXPERIMENTAL SECTION

A commercial Al foil (50 μm thick, Aldrich) was laminated into a poly(ethylene naphthalate) (PEN) film (188 μm thick, SKC) via a roll-to-roll procedure. Some of these foils were directly used as gate electrodes (18). The surface of other laminated Al foils was smoothly polished by electrolytic etching. For comparison, a 5 μm thick Al layer was sputtered onto a heavily doped Si

* Corresponding author. Tel: +82-32-860-7494 (H.Y.); +82-54-279-2269 (C.E.P.). E-mail: hcyang@inha.ac.kr (H.Y.); cep@postech.ac.kr (C.E.P.).
† Inha University.
‡ Pohang University of Science and Technology.

Table 1. Surface Characteristics of PAMS/Al$_2$O$_3$ Gate Dielectrics

dielectric	gate electrode	substrate	C_i (nF cm^{-2})	R_q (nm)
I	untreated Al foil	PEN	82.3	>40 nm
II	etched Al foil	PEN	77.1	0.94 $\pm$ 0.2[a]
III	sputtered Al	Si	76.7	0.93 $\pm$ 0.1

[a] This R_q value was calculated from the nanoscale features, excluding the micrometer-sized dimples, which cover 5−15% of the surface area.

substrate and further polished to generate a flat gate-electrode surface. Al oxide (Al$_2$O$_3$) layers on these Al gate electrodes were prepared by anodizing the films in 0.1 M ammonium pentaborate octahydrate solution. Bilayer type gate dielectrics were then finalized by spin-casting a 1.0 wt % PAMS (molecular weight = 9000 g/mol) solution (in toluene) onto the Al$_2$O$_3$ layers. Pentacene films were deposited on the PAMS/Al$_2$O$_3$ gate dielectrics held at room temperature, under a vacuum pressure of ~1 × 10^{-7} Torr with a deposition rate of 0.3 Å s^{-1}. Top-contact Au electrodes were patterned onto the pentacene films through a shadow mask.

The capacitance (C_i) of each gate dielectrics was measured with an HP 4284A Precision LCR meter. Using Keithley 2400 and 236 source/measurement units, the electrical performances of the pentacene-FETs were measured without tensile strain (ε) or with a fixed ε to demonstrate their deformation stability. Values for μ_{FET} were calculated from the drain-source current (I_{DS})−gate voltage (V_G) transfer curves of the OFET devices operated in the saturation regime, by fitting to the following equation

$$I_{DS} = \left(\frac{WC_i}{2L}\right)\mu_{FET}(V_G - V_T)^2$$

where L is the channel length, W is the channel width, and V_T is the threshold voltage.

The dielectric R_q-dependent pentacene nanostructures were characterized by AFM (Multimode Nanoscope IIIa, Veeco) and synchrotron-based X-ray diffractions (X21, National Synchrotron Light Source, Brookhaven National Laboratory). In addition, CP-AFM current mapping was performed simultaneously with contact AFM imaging for 5 nm thick pentacene films in direct contact with the gate dielectrics, as described previously (7, 11).

3. RESULTS AND DISCUSSION

PAMS/Al$_2$O$_3$ bilayer dielectrics, manipulated on untreated or electrolytically etched Al-foil/PEN substrates, were fabricated in an effort to realize low-cost and flexible pentacene-OFETs. The pentacene crystal structures on the charge transport behavior of the dielectrics were compared to the properties of flat PAMS/Al$_2$O$_3$ dielectrics generated from a sputtered Al/Si substrate. Table 1 shows the characteristics of the PAMS/Al$_2$O$_3$ dielectrics based on three different types of Al gate-electrodes. The overall surface energy (γ) values for the gate dielectrics were in the range 34.7−37.5 mJ m^{-2}, as calculated from the surface contact angles of water and dimethylformamide (10−12). These values were similar to those of the PAMS film alone, 36.9 mJ m^{-2}, suggesting that the spin-cast PAMS layers almost completely covered the relatively hydrophilic Al$_2$O$_3$ surfaces.

Figure 1 shows AFM surface topographies of the PAMS/Al$_2$O$_3$ dielectrics. AFM measurement over eleven different

3 × 3 μm^2 area on each dielectric allowed evaluation of the surface roughness. PAMS films spin-cast to a thickness of 10−15 nm tended to mimic, at the surface, the intrinsic textures of the bottom Al$_2$O$_3$/Al surfaces. In particular, the PAMS layer did not completely cover the Al$_2$O$_3$ layer grown from the untreated Al foil with mechanical grooves (Figure 1a). As a result, the value of R_q for the PAMS/Al$_2$O$_3$ gate-dielectric, referred to as dielectric **I**, was >40 nm. Electrolytic etching of the Al foil surface produced a bilayer gate dielectric (dielectric **II**) with an R_q of 0.94 nm (with the exception of the lateral μm-sized dimple area, Figure 1b), which was similar to the R_q for the dielectric formed on a flat 5 μm thick sputtered Al/Si, dielectric **III**.

In pentacene-OFETs, the crystalline structure of the first few monolayers that contact the gate dielectrics plays an important role in the charge carrier transport (7). Figure 2 shows AFM topographs of 5 and 50 nm thick pentacene films on each type of bilayer gate dielectric. On the bilayer dielectric **I** (R_q > 40 nm), irregular pentacene islands generated by an island growth mode did not form a percolating network in 5 nm thick film (Figure 2a), although 50 nm thick pentacene film did show a percolating network of crystal islands (Figure 2d). By comparing the pentacene crystals on the PAMS-covered and -dewetted Al$_2$O$_3$ area, we found that the bilayer gate dielectric employing hydrophobic PAMS induces larger crystal grains (see Figure 2a,d). The larger grain property resulted from the γ and R_q for the PAMS-covered area, which were lower than the open Al$_2$O$_3$ surface.

Unlike dielectric **I**, which was characterized by a coarse and heterogeneous surface, the fine dielectric surfaces (R_q < 1 nm) from both etched Al (dielectric **II**, except for micrometer-sized surface dimple area) and sputtered Al gates (dielectric **III**) induce terracelike crystals with a layer by layer island growth mode. AFM was generally unable to resolve the pentacene nanostructures within the micrometer-sized dimple areas of bilayer dielectric **II**. Therefore, CP-AFM result obtained from regions around these dimple areas will be discussed later in this paper.

The charge transport behavior of these pentacene films was determined by patterning top-contact Au electrodes on 50 nm thick pentacene films (Figure 3a). Figure 3b and Table 2 show I_{DS}−V_G transfer curves and electrical characteristics, respectively, of pentacene-OFETs operated in the saturation regime ($V_{DS} = -6$ V). The etched Al-foil based dielectrics (dielectric **II**) showed $\mu_{FET} \approx 0.39$ cm^2 V^{-1} s^{-1} and $I_{on}/I_{off} \approx 1 \times 10^6$. Although the conducting paths for charge carrier transport contained undulations due to the localized dimples on the dielectric surface, the hole mobility was vastly superior to that of the untreated Al-foil based samples, device **I** ($\mu_{FET} = 0.15 \pm 0.09$ cm^2 V^{-1} s^{-1}). Note that the large variation in μ_{FET} of device **I** was attributed to the presence of PAMS-dewetted area on the PAMS/Al$_2$O$_3$ dielectric, inducing heterogeneous grains of pentacene crystals (see Figure 2a,d). The value of μ_{FET} for device **II** was similar to that ($\mu_{FET} \approx 0.40$ cm^2 V^{-1} s^{-1}) of the reference device **III** on dielectric **III** (R_q < 1 nm). These device characteristics suggest that control of the nanoscale interface between the semiconduc-
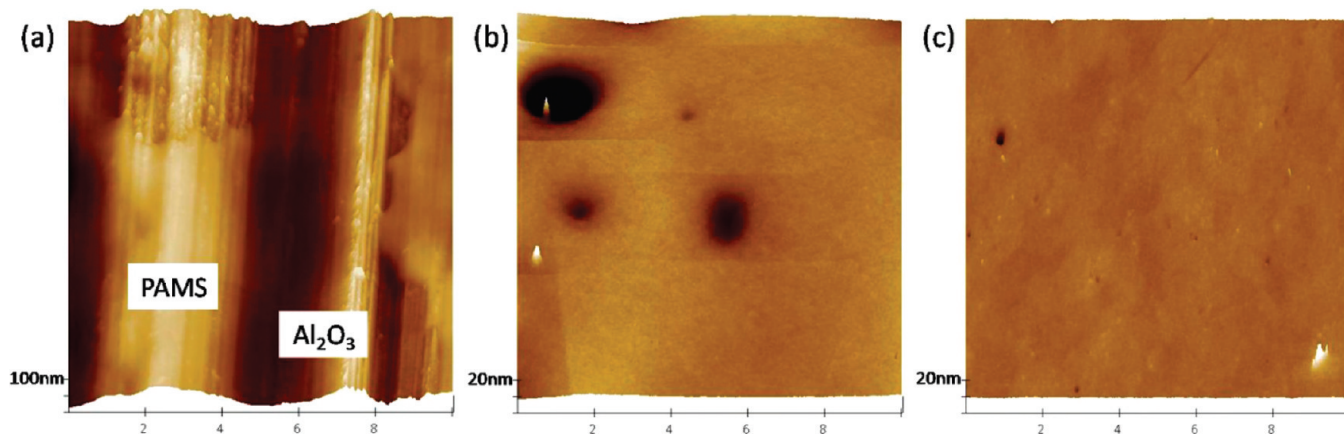
FIGURE 1. AFM topographs of the PAMS/Al$_2$O$_3$ gate dielectrics on (a) untreated Al foil (I), (b) etched Al foil (II), and (c) sputtered Al-based gates (III). (In b, lateral micrometer-sized dimples with a height of 80−280 nm cover 5−15% in the dielectric surface.)
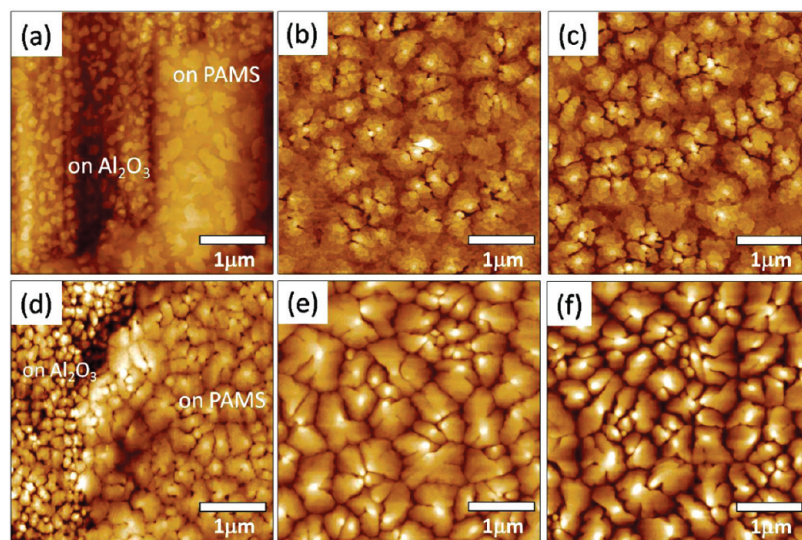

FIGURE 2. AFM topographs of (a−c) 5 and (d−f) 50 nm thick pentacene films on the PAMS/Al$_2$O$_3$ dielectrics based on (a, d) untreated Al foil (dielectric I), (b, e) etched Al foil (dielectric II), and (c, f) sputtered Al (dielectric III).
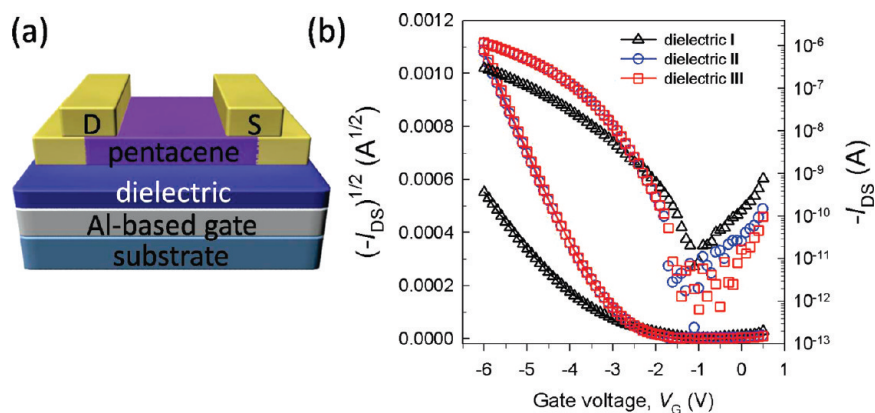

FIGURE 3. (a) Schematic diagram of the pentacene-OFET geometry ($L = 150\,\mu$m and $W = 1500\,\mu$m). (b) I_{DS}−V_G transfer curves for the pentacene-OFETs based on different types of Al gate electrodes.

tor/gate-dielectric plays an important role in the lateral transport of charge carriers.

Two-dimensional (2D) X-ray analysis for crystalline thin films, in which both parallel and vertical crystal reflections are collected, is a powerful tool for the characterization of crystalline structures and variations in crystal orientation present in a surface (7). 2D grazing-incidence X-ray diffrac-

tion (GIXD) and X-ray rocking scan were collected for 5 and 50 nm thick pentacene films, respectively, to systematically investigate effects of the dielectric surface roughness on the crystalline structures of pentacene. As shown in Figure 4a−c, 2D GIXD patterns for the 5 nm thick pentacene films confirmed that most pentacene grains, on the three different gate dielectrics, contained a "thin film phase" of "edge-on" mo-
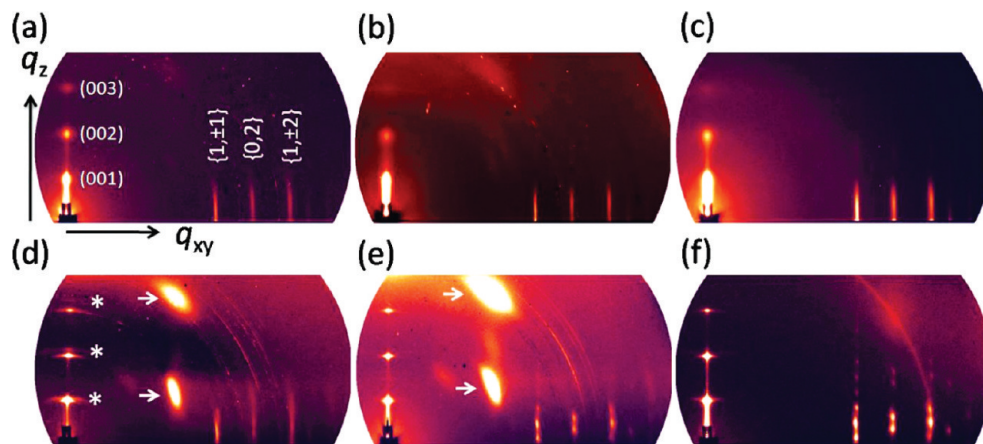
FIGURE 4. (a–c) 2D GIXD patterns of 5 nm thick pentacene films and (d–f) X-ray rocking patterns of 50 nm thick pentacene films on (a, d) untreated Al foil (dielectric I), (b, e) etched Al foil (dielectric II), and (c, f) sputtered Al-based (dielectric III) gate dielectrics. (The peaks marked with white arrows in d and e are related to the X-ray reflections of the Al substrates.)

Table 2. Electrical Performances of Pentacene-OFETs with PAMS/Al$_2$O$_3$ Dielectrics Based on Various Types of Al Gates

device	base gate	μ_{FET} (cm^{2}V^{-1}s^{-1})	I_{on}/I_{off}	V_T (V)	SS (V dec^{-1})
I	untreated Al	0.15 ± 0.09	1×10^4 to 1×10^5	-3.43 ± 0.14	0.28 ± 0.15
II	etched Al	0.39 ± 0.01	$\sim 1 \times 10^6$	-3.08 ± 0.17	0.17 ± 0.07
III	sputtered Al	0.40 ± 0.01	$\sim 1 \times 10^6$	-3.17 ± 0.10	0.16 ± 0.05

lecule with an interlayer spacing of 15.1 Å (7, 11–13, 19–21), independent of the macrocrystalline morphologies, i.e., discrete islands or percolated layers. Unlike the percolated pentacene layers, however, discrete pentacene islands (8–12 nm in height) on the dielectric **I** show much stronger Bragg rod reflections in the out-of-plane direction, q_z, because of the presence of additional stacked layer formation (7).

X-ray rocking scan determines the average orientation of all crystals in a thin film. As shown in Figure 4d–f, the X-ray rocking scans identified the sample-to-sample differences in crystal orientation, specifically along the q_z, direction, in 50 nm thick pentacene films. Figure 5 shows the out-of-plane X-ray profiles extracted from the rocking scans. The 2D patterns of the samples on both the dielectric **II** and **III** ($R_q \approx 1$ nm) exhibited strong out-of-plane X-ray reflections originating from the "thin film phase" with a multilayered structure (Figure 4e,f). In contrast, the X-ray result for the sample on the dielectric **I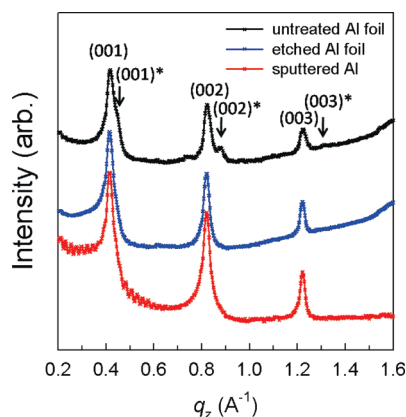** confirmed that the pentacene film contained large portions of a "bulk phase" with a layer spacing of 14.5 Å, as well as the "thin film phase" (see the peaks marked with asterisks in Figures 4d and 5). In addition, two polymorphic crystals were oriented away from the film surface, as indicated by broad X-ray reflections along Debye rings. This result arose from a structural misalignment between the initial pentacene islands and the second generation crystals formed on the irregular and coarse surface. Furthermore, the second-generation crystals contained large portions of "bulk phase".

Hole transports in pentacene polymorphs is supported mainly by π-orbital overlaps along the in-plane *ab* direction, which provide conducting paths, because the overlap is negligible along the *c*-axis, i.e., between crystal layers (22). Additionally, herringbone molecular packing produces discernible charge transport along face-to-face and face-to-edge pathways via intermolecular π-orbital overlaps. The triclinic "bulk phase" polymorphic phase, with more tilted molecular orientations, yields reduced π-orbital overlap. In device **I**, which contained "bulk phase" and a broad distribution of crystal orientations, the threshold voltage (V_T) was shifted to more negative values and the high subthreshold slope (*SS*) (Figure 3b and Table 2) As a result, the structural mismatch by the coexistence and percolation of the island-type crystal phases, i.e., static disordered, limited charge transport, and significantly contributed to the degradation of the corresponding OFETs.

CP-AFM characterizes the lateral charge transport along polycrystalline grains (7, 11, 23, 24). The hole mobility of the device **II** is identical to that ($\mu_{FET} \approx 0.40$ cm^2 V^{-1} s^{-1}) of the device **III**, although the conducting paths undulated due to the localized dimples on the dielectric **II**, CP-AFM was performed for the 5 nm thick pentacene films on each
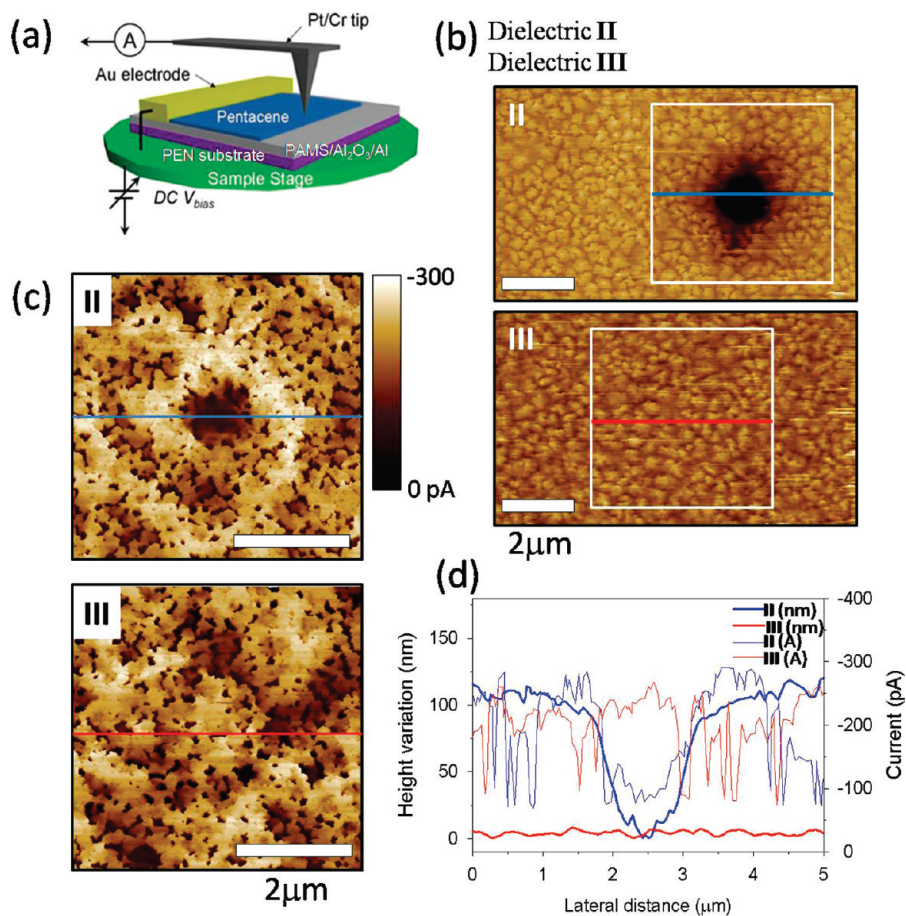

FIGURE 5. Out-of-plane X-ray profiles extracted from the rocking patterns of the 50 nm thick pentacene films.

FIGURE 6. (a) Schematic diagram of the CP-AFM experiment. (b) Contact-AFM topographs of 5 nm thick pentacene films on the dielectric **II** and **III**. (c) CP-AFM current images of the areas in the white boxes in b, as collected at $V_{bias} = 2$ V. (d) Cross-sectional height and current profiles.

dielectric, as shown in Figure 2a−c (11). Under a fixed bias (V_{bias}) applied through the top Au electrode grounded by the bottom AFM steel disk, the lateral currents in the local film area (near the electrode) were measured using a Pt/Cr-coated AFM probe (Figure 6a). All CP-AFM currents, which were monitored simultaneously during contact-AFM topography, were normalized with respect to the dark currents at $V_{bias} =$ 0. The currents present in the discrete pentacene islands on the coarse dielectric **I** were below the detectable current limit of CP-AFM (<1 pA). The 5 nm thick pentacene films on the dielectric **II** and **III** showed, by CP-AFM current images, a continuous current flux of 200 ± 100 pA, which varied according to the grain boundaries (GBs) and the scan area (Figure 6c). As shown in Figure 6d, the lateral conductance slightly decreases across GBs and inside dimples (e.g., for widths of 1.5 μm and depths of 100 nm). In contrast, the current variation across the edges of the dimples was not significantly different from the variations across the GBs of the flat dielectric surfaces (dielectric **III**). The CP-AFM results for the pentacene films on the dielectric **II** and **III** showed that the presence of the microscale curvature on local dielectric surface did not hinder self-organization of the seeding pentacene if the contact interface between penta-cene and the dielectric was controlled on the nanoscale.

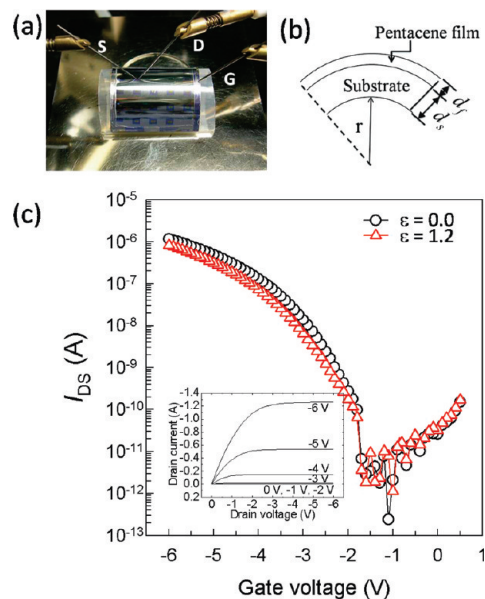The performance stability of the pentacene-FETs with the PAMS/Al$_2$O$_3$ dielectrics that had been mounted on flexible

FIGURE 7. (a) Digital camera image of the $I−V$ measurement setup for a given ε. (b) Schematic diagram of a pentacene-OFET bent with an inner radius r. (c) ε-dependent $I_{DS}−V_G$ transfer curves of penta-cene-OFETs based on etched Al foil-based dielectrics.

substrate were tested under bending conditions. Figure 7a shows a digital camera image of the device under an actual $I−V$ measurement setup. An analytical solution for the

tensile bending strain was obtained based on the model shown in Figure 7b. If an organic thin film coated on a flexible substrate is bent at an inner radius r, a tensile bending strain (ε) arises at the outer surface of the film as described by (25, 26)

$$\varepsilon = \frac{(d_f + d_s)}{2r} \qquad (2)$$

where d_f (= 50 nm) and d_s ($\sim$ 240 μm) are the thicknesses of the film and substrate, respectively. The inner radius r is controlled by mounding the pentacene-OFETs on split plastic tubes of different radii.

Under a given ε, the average value of μ_{FET} remains over 80% ($\sim$0.32 cm^2 V^{-1} s^{-1}) of μ_{FET} for the same device **II** at ε = 0, up to ε = 1.2%, as calculated from the I_{DS}–V_G transfer curves (Figure 7c). The experimental correlations between dielectric R_q and pentacene nanostructures, combined with the correlations between CP-AFM current and μ_{FET}, indicate that bilayer gate-dielectric fabrication using Al foil is sufficiently robust and reproducible for the fabrication of flexible high-performance OFETs.

4. CONCLUSION

Smooth polymer/Al$_2$O$_3$ bilayer gate dielectrics were fabricated on a commercial Al foil that had been laminated on a flexible polymer substrate by the following procedures: electrolytic etching, anodizing of the Al, and spin-casting poly(α-methyl styrene) (PAMS). The PAMS/Al$_2$O$_3$ dielectric had a surface roughness of R_q < 1 nm, although isolated micrometer-sized dimples were present on the dielectric surface because of the intrinsic mechanical grooves of the Al foil surface. CP-AFM and X-ray diffraction characterization of 5 and 50 nm thick pentacene films grown on gate dielectrics at room temperature showed that highly percolated terracelike crystals of "edge-on" pentacene molecules were present on the flat sputtered Al-based dielectrics. 50 nm thick pentacene-FETs on the flexible dielectric/gate substrate exhibited a μ_{FET} value of $\sim$0.39 cm^2 V^{-1} s^{-1}, which was comparable to values for devices that had been developed on flat PAMS/Al$_2$O$_3$ dielectrics. In particular, the average value of μ_{FET} in the pentacene-FET under bending condition ($\varepsilon \leq 1.2$) remained above 80% of the μ_{FET} for the same device operated at ε = 0. In addition, this value was higher, by a factor of 2.5, than that of pentacene-FETs based on PAMS/Al$_2$O$_3$ dielectrics from Al foil without electrolytic etching (R_q > 40 nm).

These results suggest that the microscale surface curvature of the gate-dielectric does not affect the crystalline nucleation and growth of pentacene in terms of the contact length scale of the seeding molecule. In contrast, nanoscale surface roughness plays an important role in self-organization at the pentacene–dielectric interface. Finally, we conclude that bilayer gate dielectric fabrication from Al foil is sufficiently robust and reproducible for the fabrication of flexible high-performance OFETs.

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